A DIGITAL CUT-OFF CONTROL LOOP FOR TV USING SPEEDING & BLANKING CIRCUITS

Field of the Invention

This invention relates to a television/video display control circuit, and in particular to a cut-off control circuit for use in a television RGB controller.

Background of the Invention

A cut-off control loop circuit in a television permits the automatic control of the cut-off point of the three RGB cathodes. The black level of the RGB signals is automatically adjusted to have the same cut-off current on each of the RGB cathodes, in order to have the proper DC level at each RGB cathode, for a correct colorimetry of low light level signals. The RGB cathode currents are sequentially measured at the output of the external video amplifier during the three cut-off lines. A conventional 8-bit digital cut-off control loop has low resolution of the black-level adjustment, requires a relatively long time to reach cut-off stability when the TV set is switched on, and cannot blank the RGB output when the cut-off control loop is not stable. To increase the resolution to 9-bits leads to even longer convergence times of the cut-off loops.

Summary of the Invention

The present invention aims to address some of the difficulties associated with the prior art, and embodiments of the invention are able to provide an increased resolution of black level adjustment whilst having a short cut-off convergence time during initialisation and enabling blanking of the RGB outputs when the cut-off control loop does not converge to the correct level.

In accordance with the present invention, there is provided an RGB control circuit for use in

television/video display control, comprising: a display driver current sensor; a counter circuit and analog output circuit coupled to control the display driver current; a speeding comparator having a plurality of comparator circuits coupled in parallel with the display driver current sensor as input, for determining and outputting a measure of the difference between the sensed display driver current and a predetermined value thereof; and a speeding logic circuit coupled to the speeding comparator and counter circuit, and arranged to control the up/down counting rate of the counter circuit according to said measure of difference in display driver current.

The speeding logic circuit may be arranged to control the counting rate of the counter circuit, and thus the display driver current, based on the output of the speeding comparator so as to efficiently converge the display driver current to the predetermined value.

Preferably the speeding logic circuit produces a RGB output blanking signal whilst said display driver current is substantially different from said predetermined value. Preferably control circuits are provided for each of the colour (RGB) channels, wherein the speeding logic circuit produces the RGB output blanking signal based on the counting rate of any and/or each of the counter circuits for the colour channels.

Preferably the speeding comparator has a plurality of outputs including a convergent output and at least one upper output and lower output, wherein the convergent output corresponds to the display driver current being substantially equal to the predetermined value and the upper and lower outputs are utilised by the speeding logic circuit to determine the up/down counting rate of the counter circuit. In an preferred embodiment, each of the upper and lower outputs correspond to respective up and down binary counting rates for the counter circuit.

Brief Description of the Drawings

The invention is described in greater detail hereinafter, by way of example only, with reference to the accompanying drawings, wherein:

Figure 1 is a block diagram of a conventional 8-bit digital cut-off control loop for one channel of an RGB output controller;

Figures 2 and 3 are waveform diagrams;

Figure 4 is a block diagram of a digital cut-off control loop for one channel of an RGB output controller, in accordance with a preferred embodiment of the present invention; and

Figure 5 is a schematic block diagram of an implementation of speeding logic and up/down counter circuitry according to an embodiment of the invention.

Detailed Description

A conventional 8-bit digital cut-off control loop circuit is shown in block diagram form in Figure 1. In the drawing, only the BLUE channel circuitry is shown, the for which the red and green channels are the same. The cut-off control loop permits the automatic control of the cut-off point of the three RGB cathodes. The black level of the RGB signals is automatically adjusted to have the same cut-off current on each of the RGB cathodes. The RGB cathode currents are sequentially measured at the output of the external video amplifier during the three cut-off lines.

During the frame blanking pulse, the RGB outputs are blanked and the total cathodes leakage current *Ileak* is measured. The cathode current is input to the circuit at *ICAT*. An external measurements resistor *Rcath* is connected between the pin *ICAT* and the ground. During the leakage current measurement the circuit provides a controlled current *Iref* so that the total current (*Iref* + *Ileak*) through the external resistor *Rcath* reaches the reference leakage voltage *Vleak*, where:

$$Vleak = (Iref + Ileak) * Rcath$$

The maximum controlled current Iref that the circuit can provide is 200uA, and it is memorized by use of an internal capacitor *Cref*. The leakage reference voltage *Vleak* is 1.75V.

The cut-off current measurement is sequentially achieved for the channels during the three lines after the frame blanking (cut-off lines), as is illustrated in Figure 2. During the first cut-off line, a reference voltage is inserted on the blue channel output, the green and the red outputs are blanked. The total cathode current is the leakage current (previously measured) plus the blue cut-off current *Icb* is then present. If the voltage on the *ICAT* pin is not equal to the cut-off reference voltage (*Vcut-off*), the simple comparator will give an up or down signal to the 8-bit up-down counter so that the output current of the 8-bit DAC will automatically change until the voltage on the *ICAT* pin is equal to *Vcut-off*. Thus the circuit can adjust automatically the black-level so that the voltage on the *ICAT* pin is equal to cut-off reference voltage (*Vcut-off*), wherein:

$$Vcut\text{-}off = (Iref + Ileak + Icb) * Rcath$$

The black level is memorized using the 8-bit up-down counter and the 8-bit DAC. The blue cut-off current is determined by the resistor *Rcath*, such that:

$$Icb = (Vcut\text{-}off - Vleak) / Rcath$$

The second cut-off line is used for the green channel cut-off adjustment (red and blue outputs are blanked) and the same manner as described above, and the last cut-off line is dedicated to the red channel cut-off adjustment (with blue and green outputs blanked). The cut-off control loop can adjust the black level in a range of 2V.

The beam current during the scanning can be relatively high, and in order to avoid high voltage on the *ICAT* pin, a clamping circuit will clamp the *ICAT* voltage to 2.5V. At the time of start-up, the circuit is in a warm-up detection mode, with waveforms similar to that illustrated in Figure 3. When the TV set is switched on, the cut-off control loop is not active, and during the three cut-off lines a white level is inserted on the RGB outputs in order to avoid a white flash on the screen at the start. As soon as the start beam current *Istart* is detected on the *ICAT* pin, the cut-off control loop becomes active and the cut-off levels are

inserted during the three cut-off lines, where:

$$Istart = (Vstart - Vleak) / Rcath \qquad Vstart = 2.3V$$

The sensing of the start beam current is achieved during a small window at the middle of the cut-off lines.

Conventional cut-off control loop circuits of the type described above and illustrated in Figure 1 have a number of drawbacks, some of which are summarised below:

1) Low resolution of the black level adjustment.
Generally, the range of the black level adjustment is about 2V. Since there is total 256 steps for the 8-bit DAC, the resolution of the black level adjustment is equal to 2/256=8mV.

2) Long cut-off convergence time when the TV set is switched on.
In a worst case, 256 steps are required for the conventional cut-off loop circuit to reach a stable state. Since the conventional circuit works at the frame frequency, the time that must be allowed for the loop circuit to reach its convergence point is about 256*1/50=5 seconds (assuming a frame frequency equal to 50HZ).

3) No RGB-output blanking is provided when the cut-off control loop is not stable.
When the cut-off control loop is not stable, the conventional circuit does not blank the RGB output. In this instance, the picture on the screen is not stable, and the colour may change. Pictures with strong colorimetry errors can therefore result.

Figure 4 is a block diagram of a digital cut-off control loop circuit for one channel of an RGB output controller, in accordance with a preferred embodiment of the present invention. Once again, in the drawing, only the BLUE channel circuitry is shown, and the red and green channel circuits will in practice be essentially the same. The circuit includes a number of

improvements over the conventional cut-off control loop circuit described above, and some of the improved features are discussed hereinbelow:

1) The simple comparator is replaced by a set of comparators (speeding comparator), indicating how far the loop is from a stable solution.

2) An additional speeding circuit is included which can generate the RGB output blanking signal while the cut-off control loop is not stable.

3) The 8-bit up-down counter is replaced by the 9-bit up-down counter.

4) The 8-bit DAC is replaced by the 9-bit DAC.

The working principle of the improved circuit is quite similar to the above described conventional circuit, however the relatively simple additional features provide very advantageous effects in overcoming or reducing the problems discussed above. The improved circuit uses a 9-bit up-down counter and a 9-bit DAC to replace the 8-bit up-down counter and the 8-bit DAC of the conventional circuit, in order to increase the resolution of the black level adjustment. Ordinarily this would result in an even longer convergence time for the loop circuit to determine a stable cut-off voltage. However, the improved circuit also employs a speeding comparator in place of the simple comparator of the prior art, and adds a speeding block to reduce the time required to reach stability when the TV set is switched on.

The speeding comparator comprises of six parallel comparators arranged with different comparison voltages spread over an operative range. The output of the speeding comparator is fed to a speeding logic circuit which is interposed between the comparator and the up-down counter. The combination of speeding comparator and logic circuit are used to reduce the convergence time of the cut-off control loop circuit. The speeding comparator produces an output which is dependant upon the level of the *ICAT* voltage within the operative range.

Based on the speeding comparator output, the speeding logic circuit produces an output to the up-down counter to vary the output thereof up or down. Depending upon how far away from the stable voltage the circuit is, as indicated by the speeding comparator output, the logic circuit instructs the counter to increase or decrease by a greater or lesser amount. The combined function of the speeding comparator and logic circuit is best illustrated in Table 1, presented below.

If the voltage on the *ICAT* pin is far away from 2V, that means the cut-off control loop is not stable, and the speeding comparator and the speeding logic circuit will therefore produce a signal to the 9-bit up-down counter to increase or decrease the output current of the cut-off control loop at 4-times the standard speed. This enables the improved cut-off control loop circuit to reach stability in a greatly reduced time, despite using a higher resolution counter and DAC. In order to avoid the need to increase the clock, the speeding is obtained by modifying the bits LSB+1 or LSB+2 of the Up/Down counter.

The speeding logic circuit also produces a RGB-output blanking signal to blank the RGB output. RGB output blanking bypasses the counter and DAC portion of the loop circuit to blank the RGB output when the cut-off control loop is not stable. The stability of the cut-off control loop is judged by the speeding logic circuit on the basis of the speeding comparator output, as discussed above. Thus, the improved circuit will blank the RGB output whilst the cut-off control loop is unstable, so the picture on the screen is not seen, which is better for TV set. This is done again, using the outputs of the comparators, as an indication of how close or far from convergence the loop is. As this information is only available during the cut-off lines, it is needed to memorize the blanking status, until the next operation of the loop.

In the improved circuit the speeding logic circuit operates to blank the RGB output if any of the three RGB channels has its cut-off loop operating at the highest counting speed (+/- 4 bits). This is a compromise between providing blanking until all 3 channels have converged (but a long blanking time), and a short blanking time (but the display of pictures with still some colorimetry errors).

Since the 8-bit DAC of the conventional circuit is replaced by a 9-bit DAC, the resolution of the black level adjustment is increased. Generally, the range of the black level adjustment is about 2V, and since, in the improved circuit, there is a total of 512 steps for the 9-bit DAC, the resolution of the resulting black level adjustment is 2/512=4mV. In worst case, when the TV set is switched on it requires 512 steps for the cut-off control loop circuit to reach a stable state. Since the cut-off control loop works at the frame frequency, the worst case stability time is therefore about 512*1/50/4=2.5 seconds. Without the speeding circuit, the worst case stability time would be 10 seconds, which is considered too long for the user.

Table 1: The function of the speeding comparator and speeding circuit

Icat input voltage (V)	Output of the Speeding Circuit
> 2.126	down 4 bits
2.046 ~ 2.126	down 2 bits
2.006 ~ 2.046	down 1 bit
1.994 ~ 2.006	stable
1.954 ~ 1.994	up 1 bit
1.874 ~ 1.954	up 2 bits
< 1.874	up 4 bits

The stable output represent a "dead zone" in order to avoid digital oscillation of the outputs, and is chosen so that at least 1 step falls inside this voltage range.

An exemplary implementation of the speeding logic and up/down counter circuitry is shown in schematic block diagram form in Figure 5, and the operation of the circuit is described hereinbelow and contrasted with the form of counter employed in the prior art applications. The circuit shown in Figure 5 includes nine counter cells which provide respective D outputs (D_0, D_1, ... , D_8) to the 9-bit DAC. In the prior art, eight cells are employed and coupled in a serial arrangement with two clocks (Ck1 for counting up and Ck2 for counting down) provided as input to the least-significant-bit cell. The cells in the improved circuit illustrated

in Figure 5 is arranged in a generally similar construction, although including nine cells as previously mentioned, and speeding logic circuitry in the form of a collection of logic gates coupled amongst the three least-significant-bit cells.

In the prior art, two clocks are provided, one for counting up and another for counting down. For counting up, the clock Ck1 is propagated as input through the counter cells on high levels (D=1), until the first low level (included). For example, for a cell A, with input $Ck1_A$ and a previous cell (A-1), with output $D_{(A-1)}$, and input $Ck1_{(A-1)}$, the following logic equation arises: $Ck1_A = Ck1_{(A-1)}$ AND $D_{(A-1)}$. An example of this counter function is expressed in the table below:

	b_0	b_1								b_n
Counter value:	1	1	.	.	1	0	X	X	X	X
Clock:	C	C	.	.	C	C	0	0	0	0
On Ck1 (in) counter becomes:	0	0	.	.	0	1	X	X	X	X

All the bits where Ck1 propagation was allowed (bits with C flag), are flipped on, creating here a +1 case. Bits with status X are unchanged.

For counting down in the prior art construction, the clock Ck2 is propagated as input through the counter cells on low levels (D=0), until the first high level (included). For example, for a cell A, with input $Ck2_A$ and a previous cell (A-1), with output $D_{(A-1)}$, and input $Ck2_{(A-1)}$, the following logic equation arises: $Ck2_A = Ck2_{(A-1)}$ AND $D_{(A-1)}$. An example of this counter function is expressed in the table below:

	b_0	b_1								b_n
Counter value:	0	0	.	.	0	1	X	X	X	X
Clock:	C	C	.	.	C	C	0	0	0	0
On Ck2 (in) counter becomes:	1	1	.	.	1	0	X	X	X	X

All the bits where Ck2 propagation was allowed (bits with C flag), are flipped, creating here

a -1 case. Bits with status X are unchanged.

For the improved speeding counter circuit of Figure 5, three up/down counting speeds are provided. To achieve this, the clock is applied at the CkX (X = 1 or 2) clock input, of cell 0 (count +/- 1 for speed 1), cell 1 (count +/- 2 for speed 2), or cell 2 (count +/- 4 for speed 4), depending of the result of the speeding comparators. A set of memory cells, 1 per comparator (not represented in the diagram) will stabilize the status before the clock pulse, in order to avoid a double clock generated by change of status during the clock pulse.

Referring to Table 1 above, the following signals can be derived from the speeding comparator outputs:

Up_1 = "up 1 bit"

Up_2 = "up 2 bits"

Up_4 = "up 4 bits"

Dn_1 = "down 1 bit"

Dn_2 = "down 2 bits"

Dn_4 = "down 4 bits"

In order to achieve the multiple speed counting, the following logic equations can be utilised:

$Ck1_0 = Clock \text{ AND } Up_0$

$Ck1_1 = (Clock \text{ AND } Up_2) \text{ OR } (D_1 \text{ AND } Ck1_0)$

$Ck1_2 = (Clock \text{ AND } Up_4) \text{ OR } (D_2 \text{ AND } Ck1_1)$

$Ck2_0 = Clock \text{ AND } Dn_0$

$Ck2_1 = (Clock \text{ AND } Dn_2) \text{ OR } (\text{NOT } (D_1) \text{ AND } Ck2_0)$

$Ck2_2 = (Clock \text{ AND } Dn_4) \text{ OR } (\text{NOT } (D_1) \text{ AND } Ck2_1)$

These logic expressions are implemented in the speeding logic circuitry coupled to the counter cells illustrated in Figure 5

An example of the counter function of the speeding counter as shown, for the case of counting

up by increments of 4, is expressed in the table below:

	b_0	b_1	b_2							b_n
Counter value:	X	X	1	.	1	0	X	X	X	X
Clock:	0	0	C	.	C	C	0	0	0	0
On Ck1 (in) counter becomes:	X	X	0	.	0	1	X	X	X	X

Where "X" states are unchanged, and the clock propagation is indicated as "C".

Another example of the counter function of the speeding counter as shown, for the case of counting down by increments of 2, is expressed in the table below:

	b_0	b_1								b_n
Counter value:	X	0	.	.	0	1	X	X	X	X
Clock:	0	C	.	.	C	C	0	0	0	0
On Ck2 (in) counter becomes:	X	1	.	.	1	0	X	X	X	X

The improved cut-off control loop circuit described hereinabove can be advantageously implemented in an integrated circuit for inclusion in TV/video RGB control circuitry, and the actual design of the circuit components will be readily ascertainable by those skilled in the art from the foregoing functional description and accompanying drawings. It will be appreciated that the improved circuit can be extended to higher bit count, or increased number of comparators for even higher counting speeds or different values of the comparators. The limitation of higher bit count then is the complexity of the DAC, which needs to be monotonous for this application.

The foregoing detailed description of the present invention has been presented by way of example only, and is not intended to be considered limiting to the invention as defined in the accompanying claims. For example, the numerical quantitites presented herein such as the

2.0 volt cut-off reference voltage and the 1.75 volt leakage reference voltage, whilst valid for the embodiment described and illustrated, do not limit the present invention to those values, and the principles and structures of the invention can equally be adapted to applications with different voltages and using different valued components.